UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,461	08/18/2003	Qi Xiang	0180144	4140

25700 7590 08/08/2006

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

EXAMINER	
NGUYEN, JOSEPH H	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/643,461
Filing Date: August 18, 2003
Appellant(s): XIANG ET AL.

Michael Farjami
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 09/26/2005 appealing from the Office action mailed on 03/03/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,190,975 KUBO et al. 02-2001

Wolf et al. "Silicon Processing For the VLSI Era", Lattice Press, vol. 1 (1986), pages 199 and 647.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 6, 9-10, 15-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Kubo et al. (US 6,190,975)

Regarding claim 1, Kubo et al. discloses in figure 1 a FET situated over a substrate 10, said FET comprising a channel 14 situated in said substrate; a first gate dielectric 19 (col. 9, lines 9-10) situated over said channel, said first gate dielectric having a first coefficient of thermal expansion; a first gate electrode 18 (col. 12, lines 64-66) situated over said first gate dielectric, said first electrode having a second coefficient of thermal expansion; wherein said first gate dielectric and said first gate electrode are selected such that a difference between said second coefficient of thermal expansion and said first coefficient of thermal expansion causes an increase in carrier mobility in said FET. (See columns 8-9)

It is noted that the first gate dielectric is made of silicon oxide and the first gate electrode made of polysilicon. Therefore, the second coefficient of thermal expansion of the first gate electrode is different than said first coefficient of thermal expansion of the first gate dielectric since the coefficient of thermal expansion depends on the material (see Exhibit A, Wolf et al.). Further, the phrase "causes an increase in carrier mobility in said FET" is merely functional language. The device of Kubo et al. naturally causes an increase in carrier mobility due to the difference of coefficients of thermal expansion of poly-silicon and silicon oxide.

Regarding claim 2, Kubo et al. discloses said second coefficient of thermal expansion is greater than said first coefficient of thermal expansion See Wolf et al.).

Regarding claim 3, Kubo et al. discloses in figure 1 said increase in said carrier mobility is caused by a tensile a tensile strain created in said channel 14.

Regarding claim 6, Kubo et al. discloses in figure 1 said FET is a PFET.

Regarding claims 9-10, 15 and 16, similar to the rejection of claims 1-3 and 6 above, Kubo et al. discloses in figure 1 all the structures set forth in the claims 9-10, 15 and 16.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 13, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubo et al. as applied to claims 1, 9 and 15 above.

Regarding claims 7, 13 and 19, Kubo et al. disclose in figure 1 substantially all the structure set forth in the claimed invention except said first coefficient of thermal expansion being greater than said second coefficient of thermal expansion. However, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify Kubo et al. by having said first coefficient of thermal expansion being greater than said second coefficient of thermal expansion to improve the performance of a FET device, since it has been held that discovering an optimum

value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

(10) Response to Argument

At the outset, on page 9, with respect to claim 1, Appellant argues Kubo et al. fails to teach, disclose or even suggest, a "first gate dielectric and a first gate electrode being selected such that a difference between the second coefficient of thermal expansion of the first gate electrode and the first coefficient of thermal expansion of the first gate dielectric causes an increase in carrier mobility in the FET device". However, as well known in the art, the coefficient of thermal expansion depends upon the material as evidence provided by Wolf et al. Kubo et al. discloses in figure 1 a FET device comprises the gate dielectric 19 is formed of silicon oxide (col. 9, lines 9-10) and the gate electrode 18 formed of polysilicon (col. 12, lines 64-66). As such, the gate dielectric has the first coefficient of thermal expansion and the gate electrode has the second coefficient of thermal expansion, and the first coefficient of thermal expansion is different than the second coefficient of thermal expansion since they are formed of different materials. Further, as explained in the rejection of claim 1 above, the phrase "causes an increase in carrier mobility in the FET" is merely functional language. The device of Kubo et al. naturally causes an increase in carrier mobility due to a difference in the coefficients of thermal expansion of polysilicon and silicon oxide.

Moreover, Appellant argues reliance on Wolf et al's teaching of coefficient of thermal expansion makes Kubo et al. an improper anticipation art reference. However, Wolf et al. is only cited to support the fact that the coefficient of thermal expansion depends upon the material, and thus Wolf et al. is provided herein as evidence only, not an applied prior art. Therefore, Kubo et al. is a proper anticipation art reference. Also, Appellant argues Wolf et al. does not teach using polysilicon as a gate electrode or any discussion of what the coefficient of thermal expansion of polysilicon is. However, Wolf et al. shows two different materials (silicon oxide and silicon) have two different coefficients of thermal expansion. From this evidence, one of ordinary skill in the art would recognize polysilicon and silicon oxide should have different coefficients of thermal expansion accordingly.

Lastly, since the rejection of claim 1 is proper, the rejection of claims 2-3, 6-7, 9-10, 13, 15-16 and 19 still stands.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Joseph H. Nguyen

Patent Examiner

Art Unit 2815

c.c

July 13, 2006.

Conferees:

KEN PARKER, SPE A.U 2815

RICKY MACK, SPE A.U 2873

FARJAMI & FARJAMI LL.P

26522 La Alameda Ave., Suite 360

Mission Viejo, CA 92691

SPE Kenneth Parker